Imperial College London

Department of Electrical & Electronic Engineering

EE2 Circuits & Systems – Mid-term Lab Oral 2024

The mid-term lab oral in the form of a 15-minutes oral examination conducted in person in Level 1 Teaching Lab. This will take place on Tuesday 5th or Wednesday 6th of November 2024. The purpose of this mid-term lab oral is to assess your level of attainment in the intended learning outcomes of **Lab 1 and Lab 2 only**. A schedule for the oral examination is attached. **This is a formal assessment.** If you are unable to attend and wish to swap with someone else, you MUST find a willing person to swap with, and seek my agreement ahead of time via email.

Logbook

You must **bring your logbook** (electronics or paper) with you to the Oral Examination. Although your logbook will NOT be formally "marked", your examiner will nevertheless assess how effective you have kept a log of the experiment and whether you have used your logbook to help you learn through planning and reflection. Your examiner will also be asking questions that can **only** be answered by referring to the logbook.

Format of the Oral – You must turn up to the Level 1 Lab at least 5 minutes before your allocated time. Your Examiner will call you over to their station when it is your turn. You will be asked questions **on Lab 1 and Lab 2 only**. The Examiner may even ask questions not directly linked to what you have done to test your **understanding**. In addition to understanding, examiner will also consider the effort you have put into completing the experiments.

Grading – Attached is the marksheet that your Examiner will be using during the oral examination. The assessment form with feedback will be returned to you via MS Teams. Your will receive a grade for this assessment according to the criteria shown below:

A = Excellent (70%+)	Completed and understood everything with no gap in knowledge
B = Good (60%+)	Completed all with good understanding with minor gaps
C = OK (50%+)	Fair understanding with some gaps, completed most parts
D = Weak (40%+)	Weak understanding with many gaps
E = Fail (below 40%).	Very weak understanding, lack evidence of real effort

We expect the average mark for this assessment to be around 65% for the entire class. To ensure fair assessment, I will perform moderation of marks between different Examiners and apply adjustments if necessary.

Learning Outcomes – Lab 1 and Lab 2

Lab 1 – Amplification

- Characterisation of signal sources with understanding of source impedance and loading effect
- Building of working op-amp circuits in a tidy manner
- Isolating load from source using op-amp using unity gain buffer
- Shifting reference voltage for single power supply operation
- Biasing input and output at middle of supply range
- AC vs DC coupling
- Gain-Bandwidth limitation of op-amp
- Interpretation of op-amp datasheet
- Multi-stage amplification
- Driving of very low output impedance (e.g. speaker) via class D amplifier

Lab 2 – Applications of Op-amps

- Rectifier circuit
- Peak detector and how to choose R C values of the detector
- Voltage comparator with hysteresis and what determines the hysteresis
- Oscillator with positive feedback, and what determines the frequency of oscillation
- Function generator and how it works
- Analogue pulse-width modulator and how it works
- Active filter using Sallen-Key topology
- Butterworth filter design

Peter Cheung

Version 1.8, 26 October 2024.

Lab Oral Schedule - (name ordered)

First name	Surname	Date	Time	Assessor
Adnan	Ahmed	Tue (5 Nov)	11.15 - 11.30	Examiner_1
Jaber	Ahmed	Tue (5 Nov)	11.30 - 11.45	Examiner_2
Tayo	Babs-Olugbemi	Wed (6 Nov)	11.15 - 11.30	Examiner_2
Benoit	Ben Moubamba	Wed (6 Nov)	11.00 - 11.15	Examiner_1
Alex	Brown	Wed (6 Nov)	10.00 - 10.15	Examiner_4
Mert	Caka	Wed (6 Nov)	09.45 - 10.00	Examiner_2
Yee	Chee	Tue (5 Nov)	10.30 - 10.45	Examiner_1
Taj	Choksi	Wed (6 Nov)	11.30 - 11.45	Examiner_3
Szymon	Ciba	Wed (6 Nov)	09.30 - 09.45	Examiner_3
Toby	Clark	Tue (5 Nov)	11.30 - 11.45	Examiner_1
Ander	Cobo Puertollanc	Tue (5 Nov)	10.00 - 10.15	Examiner_1
Jay	Dong	Wed (6 Nov)	10.30 - 10.45	Examiner_4
Matthew	Dooley	Wed (6 Nov)	11.00 - 11.15	Examiner_3
Kiron	Dutton	Tue (5 Nov)	10.45 - 11.00	Examiner_1
Dhruba	Fahmiduzzaman	Wed (6 Nov)	11.45 - 12.00	Examiner_2
Santos	Garcia Valls	Wed (6 Nov)	10.30 - 10.45	Examiner_1
Ava	Gifford-Moore	Tue (5 Nov)	11.30 - 11.45	Examiner_4
Maciej	Grzegorczyk	Wed (6 Nov)	10.15 - 10.30	Examiner_2
Ashis	Gurung	Tue (5 Nov)	09.45 - 10.00	Examiner_1
Harry	Hill	Wed (6 Nov)	10.00 - 10.15	Examiner_3
Yuki	Hoshino	Wed (6 Nov)	10.30 - 10.45	Examiner_3
Sam	Hussey	Wed (6 Nov)	10.15 - 10.30	Examiner_3
Hyo	Hwang	Tue (5 Nov)	11.00 - 11.15	Examiner_2
Mikhail	Ischenko	Wed (6 Nov)	10.15 - 10.30	Examiner_4
AHMAD	Jalloh	Wed (6 Nov)	10.00 - 10.15	Examiner_1
Dillon	Jayasinghe	Tue (5 Nov)	11.00 - 11.15	Examiner_3
Krish	Jindal	Wed (6 Nov)	11.00 - 11.15	Examiner_2
Faris	Kebire	Wed (6 Nov)	11.45 - 12.00	Examiner_1
Hisham	Khatib	Tue (5 Nov)	11.45 - 12.00	Examiner_3
Lia	Kommata	Wed (6 Nov)	09.30 - 09.45	Examiner_2
Ang	Li	Wed (6 Nov)	11.00 - 11.15	Examiner_4
Angeline	Lin	Wed (6 Nov)	11.15 - 11.30	Examiner_1
Zhiyuan	Liu	Wed (6 Nov)	09.30 - 09.45	Examiner_1
Enid	Maci	Wed (6 Nov)	11.30 - 11.45	Examiner_1
Sami	Marouf	Wed (6 Nov)	11.45 - 12.00	Examiner_4
Lily	Martin	Wed (6 Nov)	11.15 - 11.30	Examiner_4
Haris	Mehmood	Tue (5 Nov)	10.45 - 11.00	Examiner_2
Yael	Miller	Tue (5 Nov)	11.45 - 12.00	Examiner_1
Aidan	Mohammed-Ali	Wed (6 Nov)	10.45 - 11.00	Examiner_1
Sam	Mueller-Menrad	Tue (5 Nov)	09.45 - 10.00	Examiner_2
Ryan	Ong	Wed (6 Nov)	10.00 - 10.15	Examiner_2
Neil	Pakrasi	Wed (6 Nov)	11.30 - 11.45	Examiner_4
George	Politis	Tue (5 Nov)	11.45 - 12.00	Examiner_2
Ali	Rabie	Tue (5 Nov)	09.30 - 09.45	Examiner_2
Rahul	Raghavan	Wed (6 Nov)	10.15 - 10.30	Examiner_1

Jaime	Rama	Tue (5 Nov)	11.30 - 11.45	Examiner_3
Dan	Rhodes	Wed (6 Nov)	11.15 - 11.30	Examiner_3
Sadig	Sadikhzada	Wed (6 Nov)	10.30 - 10.45	Examiner_2
Nabiha	Saqib	Wed (6 Nov)	10.45 - 11.00	Examiner_2
Sachin	Sathiyaamoorthy	Tue (5 Nov)	11.15 - 11.30	Examiner_3
Luke	Scully	Wed (6 Nov)	10.45 - 11.00	Examiner_4
Yassine	Serrhini	Tue (5 Nov)	10.30 - 10.45	Examiner_2
Aditya	Sreekumar	Wed (6 Nov)	09.45 - 10.00	Examiner_4
Iheanyichukv	Stanley	Tue (5 Nov)	10.45 - 11.00	Examiner_3
Frank	Sun	Tue (5 Nov)	10.15 - 10.30	Examiner_1
Alfred	Sweet	Tue (5 Nov)	10.30 - 10.45	Examiner_3
Sean	Tam	Tue (5 Nov)	09.30 - 09.45	Examiner_1
Mickey	Techachokwiwat	Tue (5 Nov)	11.15 - 11.30	Examiner_2
Edgar	Teh	Wed (6 Nov)	10.45 - 11.00	Examiner_3
Ruizhu	Tian	Wed (6 Nov)	09.45 - 10.00	Examiner_1
Tara	Venkatesam	Tue (5 Nov)	10.15 - 10.30	Examiner_2
Scott	Verdin	Wed (6 Nov)	11.30 - 11.45	Examiner_2
Arjun	Vijayanand	Tue (5 Nov)	10.00 - 10.15	Examiner_2
Ahmad	Wahab	Tue (5 Nov)	11.45 - 12.00	Examiner_4
Chenxuan	Xi	Tue (5 Nov)	11.00 - 11.15	Examiner_1
Wei	Xu	Wed (6 Nov)	09.45 - 10.00	Examiner_3
Louis	Yong	Wed (6 Nov)	09.30 - 09.45	Examiner_4

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EE2 Circuits and Systems Module
Mid-term Lab Oral

Name of Student:

Names of Assessors:

Date: Tue / Wed

Performance on the Lab Experiments

1. Logbook Quality and Effectiveness

Highly effective | Effective | OK | Weak | Poor

2. Ability to answer questions from the logbook

Excellent | Good | OK | Poor | Very poor

3. Effort to completing Lab 1 & 2

Fully engaged Strong evidence	Good engagement Good evidence	Acceptable Engagement	Below expected Engagement	V. poor Engagement

Understanding and Learning Outcomes

4. Explanation on theories behind experiments

Excellent | Good | OK | Poor | Very poor

5. Examiner's opinion on candidate's depth of understanding in general

Broad & deep | Good | Average | Less than average | Poor

FEEDBACK TO STUDENT: **Grade:**